Le support de l'étude est une caméra embarquée dont le déplacement et le pilotage peuvent être réalisés à distance via une radiocommande ou un Smartphone.

Exercice 1 : Chaîne d'acquisition d'un joystick de manette radiocommandée

Le schéma proposé de la chaîne d'acquisition d'une manette radio-communicante de type Spektrum DX8 est donné en figure n°1 :

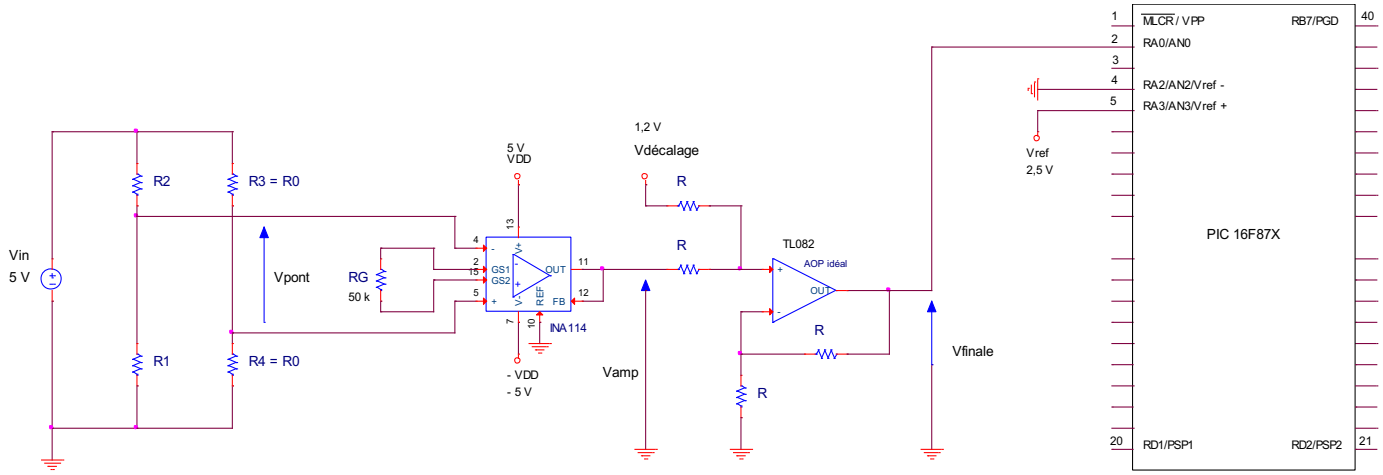


Figure 1

On se propose d'étudier le fonctionnement du joystick de la manette radio-communicante dont la documentation technique se trouve en **annexe 1**.

Il s'agit de valider la structure de la chaîne d'acquisition au regard de la sensibilité souhaitée, des conditions d'utilisation (variation de la température) et des contraintes de numérisation au niveau du microcontrôleur.

Il s'agit également de valider le choix du convertisseur analogique numérique au regard de ses performances.

R_1 et R_2 sont les résistances caractéristiques du joystick de la manette radiocommandée.

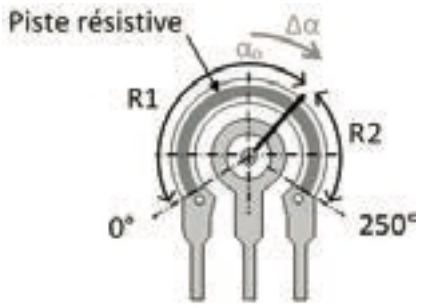


Figure 2

On notera R_0 la valeur médiane de l'élément résistif lorsque que le joystick se trouve au repos de sa position médiane $\alpha_0 = 125°$, le relevé des variations angulaires $\Delta\alpha = \pm 125°$ étant réalisé à partir de cette dernière.

1 Calculer l'expression littérale de la tension $V_{\frac{\partial s}{\partial \alpha}}$ en sortie du conditionneur en fonction de α_0 et $\Delta\alpha$ et montrer que la sensibilité de l'ensemble $\frac{\partial s}{\partial \alpha}$ est constante. Justifier l'intérêt de ce montage au regard de ce critère par rapport à une structure en pont diviseur réalisée à partir de R_1 et R_2.

Les données ont été relevées à la température nominale T_0 de 15°C. La variation de la température extérieure ainsi que l'échauffement par effet joule font évoluer la résistivité des résistances selon la loi $\rho(T) = \rho_0\left(1 + c_0\left(T - T_0\right)\right)$ où ρ_0 la résistivité du métal et le coefficient de température c_0 sont pris à la température nominale T_0. Les températures sont exprimées en °C.

2 Cette loi d'évolution de la résistivité pouvant à priori entraîner une dérive, montrer que ce montage permet de considérer que la température n'intervient pas comme facteur d'influence du montage.

La tension V_{pont} en sortie du pont n'étant pas référencée par rapport à la masse, on utilise cette tension comme entrée du composant INA114 afin de l'exploiter.

3 À partir de la documentation technique **annexe 2** du INA114, démontrer l'expression $V_{amp} = \left(1 + \frac{2R}{R_G}\right)V_{pont}$ en fonction de V_{pont}, des résistances internes R de 25 kΩ et de la résistance ajustable R_G.

4 Démontrer que le pont de Wheastone introduit une tension de mode commun liée à l'alimentation.

5 Démontrer que le premier étage de l'INA114 ne génère pas d'erreur de mode commun.

6 À partir de la documentation technique du INA114, démontrer l'expression $V_{amp} = A_d V_d + A_{cm} V_{cm}$ en fonction de la tension différentielle V_d, de la tension de mode commun V_{cm} de l'INA114, où A_d est l'amplification différentielle et A_{cm} est l'amplification de mode commun. Calculer la valeur de A_d.

7 Calculer la valeur de A_{cm} en utilisant la valeur constructeur du taux de réjection $CMRR$. Montrer que le $CMRR$ est excellent uniquement sur une bande passante limitée et que cela pose un problème si un mode commun HF est présent.

8 Donner la formule littérale du signal V_{finale} en fonction de V_{amp} et $V_{decalage}$. À partir des informations fournies dans le document **annexe 1**, calculer les valeurs extrêmes prises par les tensions V_{pont} et V_{amp}. Donner la plage de variation de la tension V_{finale}. Justifier alors l'ensemble de la structure de mise en forme compte tenu de l'exploitation faite par le signal dans la chaîne de mesure globale et des caractéristiques du convertisseur analogique numérique interne au microcontrôleur 16F877 dont vous trouverez des extraits de documentation technique **annexe 3**.

Exercice 2 : Conversion analogique numérique

Cette partie étudie le convertisseur analogique numérique mis en œuvre et qui est alimenté sous 5 V. On s'intéressera plus particulièrement au rapport signal sur bruit afin de vérifier l'efficacité de la conversion. La résolution du convertisseur permet de considérer le pas de quantification q comme suffisamment faible par rapport au signal d'entrée. On peut aussi considérer que le bruit de quantification possède une densité de probabilité uniforme.

Considérant que la caméra fait des allers retours, le signal en entrée du convertisseur est le suivant :

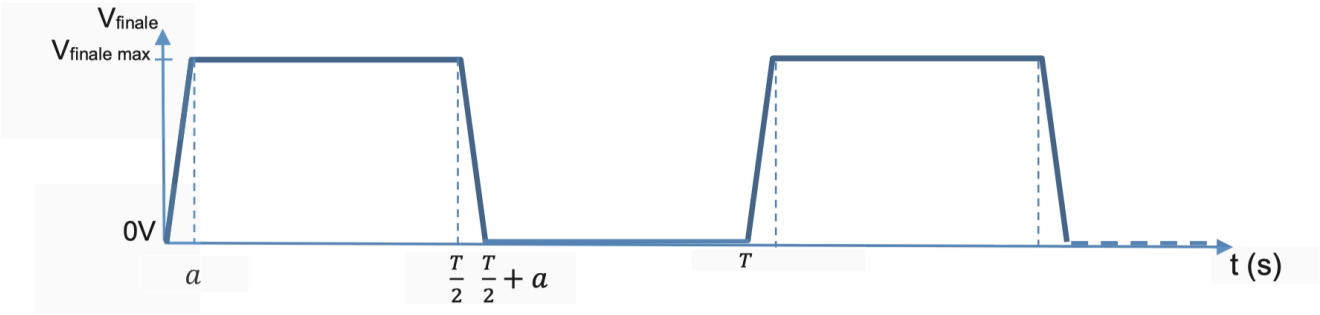


Figure 2 :

1 Donner la plage de variation de l'erreur de quantification en fonction de q. En représenter les dix premières occurrences de la plage de variation du signal d'entrée sur le **document réponse**. Calculer la puissance moyenne du signal d'erreur en fonction du quantum et en déduire la valeur efficace du bruit de quantification. Donner l'expression littérale de la valeur efficace de ce signal d'entrée en fonction des variables aT et $V_{finalmax}$. En déduire le rapport signal sur bruit en dB et faire l'application numérique si on considère que a = 1,5 s, T/2 = 24 s et $V_{finalmax}$ = 2,5 V. Indiquer comment le rapport signal sur bruit du convertisseur intégré au microcontrôleur peut être optimisé grâce au signal Vref+.

2 On considère pour cette question que l'impédance de sortie du TL082 est négligeable. À partir des indications fournies dans **l'annexe 3** du microcontrôleur, calculer le temps nécessaire à l'acquisition d'un échantillon puis le temps nécessaire entre deux conversions analogiques numériques. On se placera dans le cas le plus défavorable avec la numérisation de la plus grande valeur possible tout en tenant compte de l'erreur relative de ½ bit. On considérera également que le PIC 16F877 subit une hausse de température de 25°C par rapport à T0 et que pour cadencer la conversion analogique numérique, on applique une division par 32 à l'horloge de 20 MHz.

3 En déduire la fréquence d'échantillonnage maximale pour réaliser une conversion analogique numérique et conclure quant à la capacité du composant dans ce contexte à remplir correctement sa fonction.

4 Indiquer la valeur des registres de configuration du microcontrôleur permettant de lancer la conversion et d'obtenir un chargement des résultats de conversion à partir du bit de poids fort, sachant que seule l'entrée RA0 devra être utilisée comme entrée analogique à convertir.

Annexe 1 :

Web Site: www.parallax.com
Forums: forums.parallax.com
Sales: sales@parallax.com
Technical: support@parallax.com

Office: (916) 624-8333
Fax: (916) 624-8003
Sales: (888) 512-1024
Tech Support: (888) 997-8267

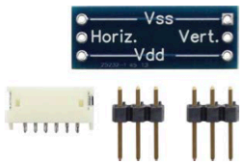
Gimbal Joystick with Adapter (#27808)

This quad-bearing gimbal joystick provides a two-axis resistive output for controlling position, velocity, tilt, etc., as an input device to various microcontrollers, including Parallax's P8X32A Propeller chip and BASIC Stamp family of modules. It may be used with microcontrollers that have analog inputs, with an external ADC, or with resistor-capacitor circuits for a purely digital solution.

The Joystick comes pre-wired with a 6-wire cable and 1.5 mm plug. An adapter kit with a matching 1.5 mm socket is included, for convenient prototyping on breadboards or thru-hole boards. Simple soldering is required to use the optional but highly recommended adapter.

Features

- 5 kΩ linear-taper potentiometer on each axis
- Smooth ball-bearing action on both axes
- Selectable spring return-to-center on vertical axis
- Selectable detents and/or friction on vertical axis
- Adapter kit for 0.1" spacing is included for easy prototyping (simple soldering required)



Specifications

- Power Requirements: Passive device; will work with any low-voltage supply
- Interface: Resistive or voltage divider output
- Dimensions: 2.70 x 2.32 x 2.42 in (68.6 x 58.9 x 61.5 mm)

Application Ideas

- Game controller
- Remote control for robotics
- Manual control for interactive displays

Packing List

- Quad-Bearing Gimbal Joystick (#27806)
- Adapter Kit (#27809) (including PCB, two 3-pin headers, and 1.5 mm 6-connector socket)

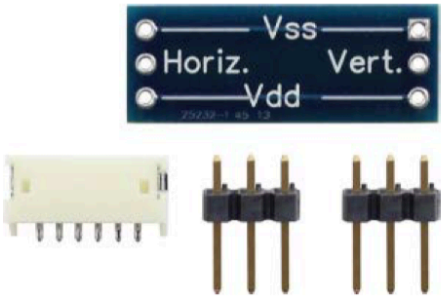
Resources and Downloads

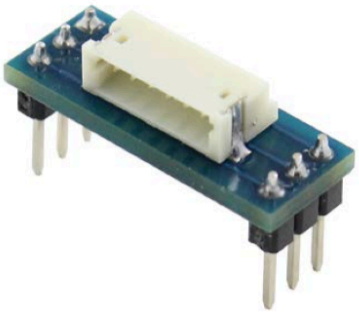
Find example code, the latest version of this document, and additional resources from the Gimbal Joystick product page. Go to http://www.parallax.com and search "27808".

Adapter Assembly

Using the adapter kit is optional but highly recommended. The example wiring photos in this document assume you are using it. The underside of the adapter board PCB is labeled as shown at left. The top of the adapter board has pads to solder the 1.5 mm socket in place, as shown at right.

(1) Put on your safety glasses!
(2) Begin by inserting the short ends of the 3-pin headers into the PCB from the underside.
(3) Solder the 3-pin headers in place from the top of the board.
(4) Solder the 1.5 mm socket in place on top of the board.

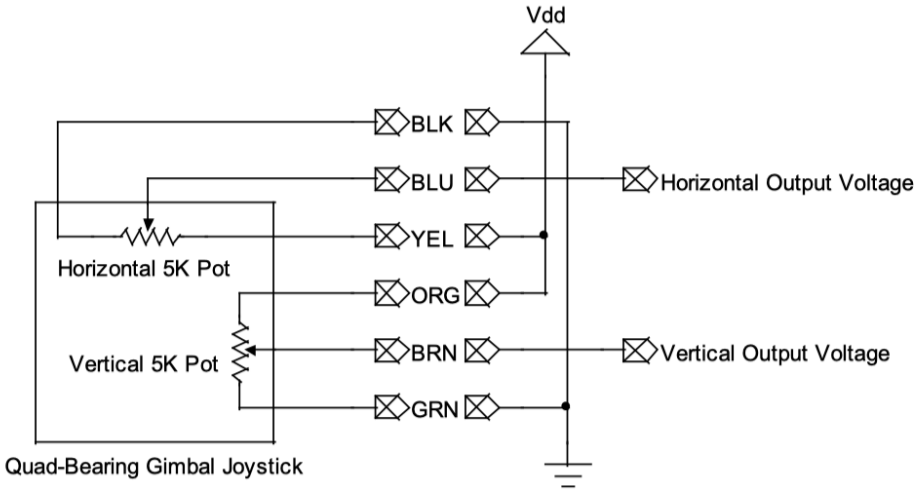




Quick-Start Guide

Voltage Divider Circuit

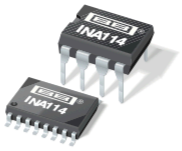
The voltage divider is most basic circuit using the joystick:



The horizontal output voltage will increase as the joystick moves from left to right, from about 0.38 * Vdd (full left) to 0.63 * Vdd (full right). The center voltage is approximately Vdd / 2. The vertical output voltage covers the same range, increasing from bottom to top, with the center voltage also being Vdd / 2.

Annexe 2 :

BURR - BROWN®



INA114

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.25μV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA max
- 8-PIN PLASTIC AND SOL-16

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

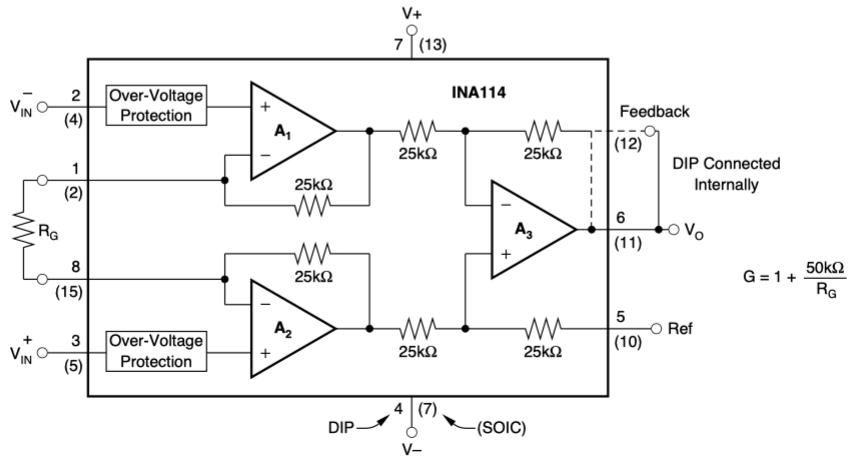
DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA114 is laser trimmed for very low offset voltage (50μV), drift (0.25μV/°C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic and SOL-16 surface-mount packages. Both are specified for the –40°C to +85°C temperature range.



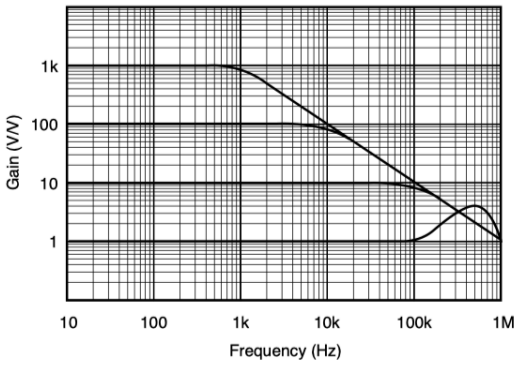
International Airport Industrial Park · Mailing Address: PO Box 11400, Tucson, AZ 85734 · Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 · Tel: (520) 746-1111 · Twx: 910-952-1111
Internet: http://www.burr-brown.com/ · FAXLine: (800) 548-6133 (US/Canada Only) · Cable: BBRCORP · Telex: 066-6491 · FAX: (520) 889-1510 · Immediate Product Info: (800) 548-6132

 PDS-1142D Printed in U.S.A. March, 1998

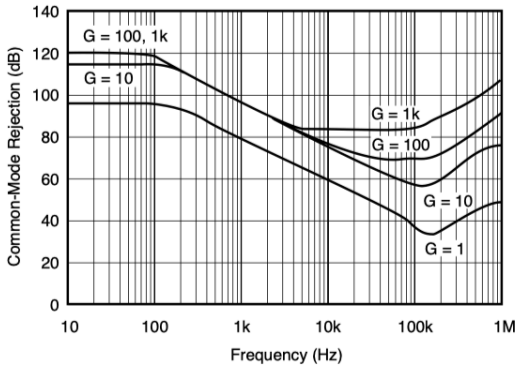
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

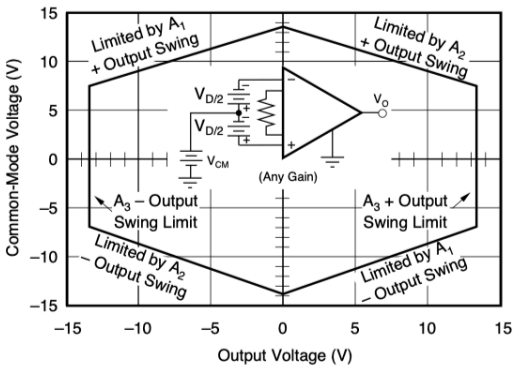
GAIN vs FREQUENCY



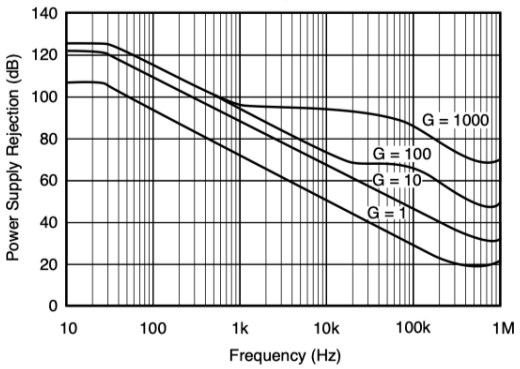
COMMON-MODE REJECTION vs FREQUENCY



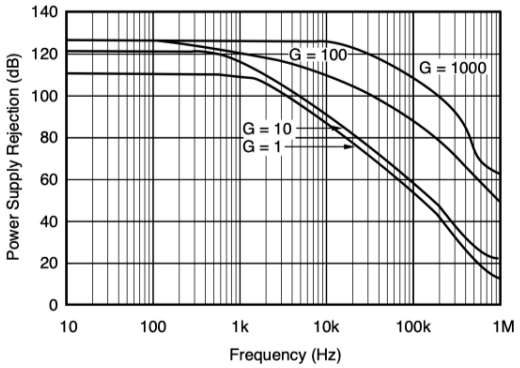
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE



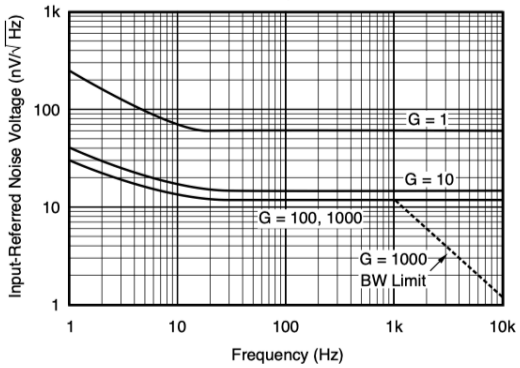
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



INPUT-REFERRED NOISE VOLTAGE vs FREQUENCY



Annexe 3 :

11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the other devices.

The analog input charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation. The A/D conversion of the analog input signal results in a corresponding 10-bit digital number. The A/D module has high and low voltage reference input that is software selectable to some combination of VDD, VSS, RA2, or RA3.

The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference), or as digital I/O.

Additional information on using the A/D module can be found in the PIC® MCU Mid-Range Family Reference Manual (DS33023).

REGISTER 11-1: ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from the internal A/D module RC oscillator)

bit 5-3 **CHS2:CHS0**: Analog Channel Select bits
000 = channel 0, (RA0/AN0)
001 = channel 1, (RA1/AN1)
010 = channel 2, (RA2/AN2)
011 = channel 3, (RA3/AN3)
100 = channel 4, (RA5/AN4)
101 = channel 5, (RE0/AN5)(1)
110 = channel 6, (RE1/AN6)(1)
111 = channel 7, (RE2/AN7)(1)

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
If ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1 **Unimplemented**: Read as '0'

bit 0 **ADON**: A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shut-off and consumes no operating current

Note 1: These channels are not available on PIC16F873/876 devices.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

PIC16F87X

REGISTER 11-2: ADCON1 REGISTER (ADDRESS 9Fh)

U-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.

bit 6-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0**: A/D Port Configuration Control bits:

PCFG3: PCFG0	AN7(1) RE2	AN6(1) RE1	AN5(1) RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ Refs(2)
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	VSS	2/1
011x	D	D	D	D	D	D	D	D	VDD	VSS	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	RA3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	RA3	RA2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	RA3	RA2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	RA3	RA2	1/2

A = Analog input D = Digital I/O

Note 1: These channels are not available on PIC16F873/876 devices.
2: This column indicates the number of analog channels available as A/D inputs and the number of analog channels used as voltage reference inputs.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The ADRESH:ADRESL registers contain the 10-bit result of the A/D conversion. When the A/D conversion is complete, the result is loaded into this A/D result register pair, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 11-1.

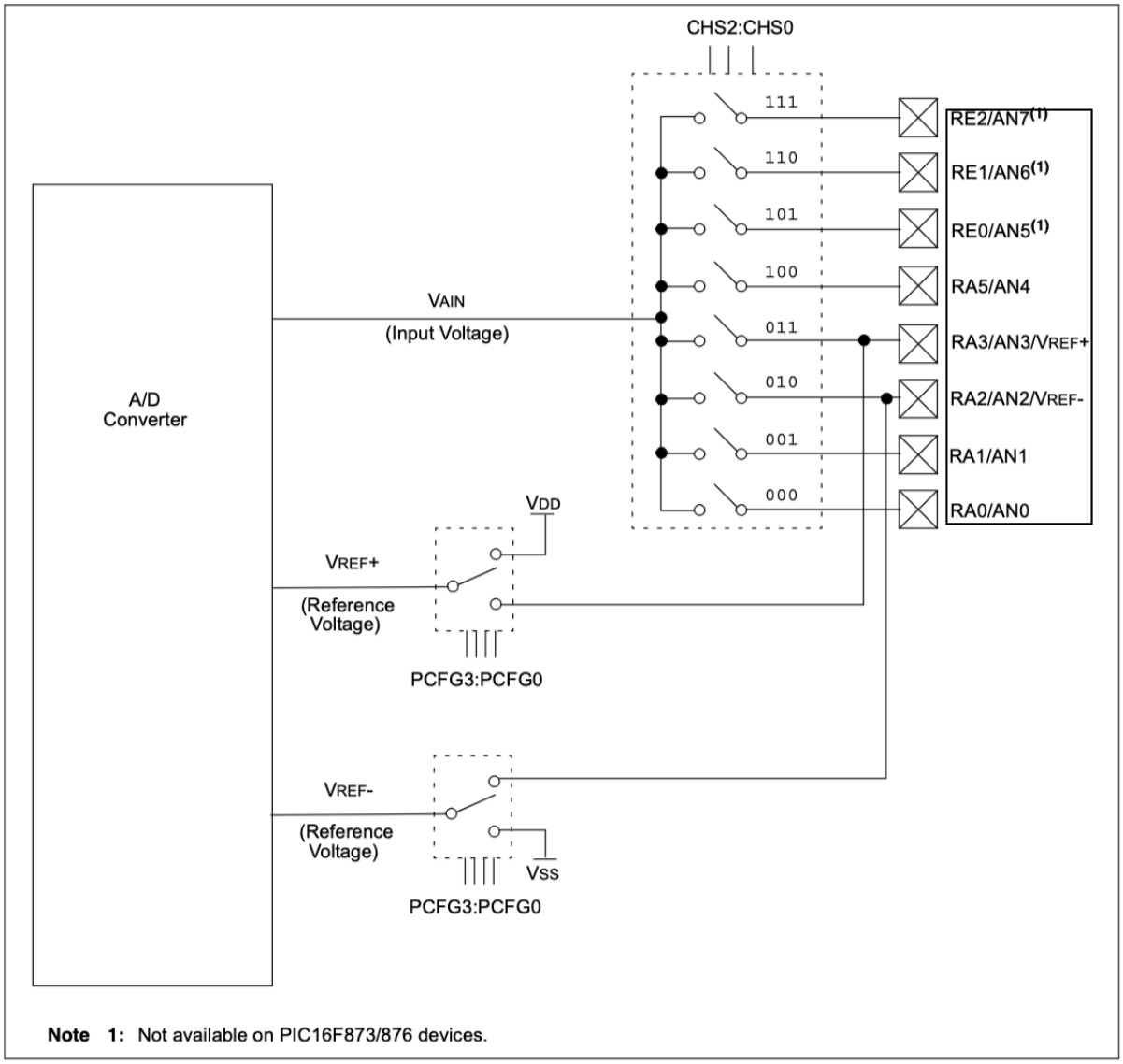
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time, see Section 11.1 on page 114. After this acquisition time has elapsed, the A/D conversion can be started.

These steps should be followed for doing an A/D Conversion:

1. Configure the A/D module:
   - Configure analog pins/voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set PEIE bit
   - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared (with interrupts enabled); OR
   - Waiting for the A/D interrupt
6. Read A/D result register pair (ADRESH:ADRESL), clear bit ADIF if required.
7. For the next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before the next acquisition starts.

FIGURE 11-1: A/D BLOCK DIAGRAM



Note 1: Not available on PIC16F873/876 devices.

PIC16F87X

11.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-2. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 11-2. **The maximum recommended impedance for analog sources is 10 kΩ.** As the impedance is decreased, the acquisition time may be decreased.

After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 11-4 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the PIC® MCU Mid-Range Reference Manual (DS33023).

EQUATION 11-1: ACQUISITION TIME

$$
\begin{aligned}
T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\
&= T_{AMP} + T_C + T_{COFF} \\
&= 2\mu s + T_C + [(\text{Temperature} - 25°C)(0.05\mu s/°C)] \\
T_C &= C_{HOLD}(R_{IC} + R_{SS} + R_S)\ \ln(1/2047) \\
&= -120pF(1k\Omega + 7k\Omega + 10k\Omega)\ \ln(0.0004885) \\
&= 16.47\mu s \\
T_{ACQ} &= 2\mu s + 16.47\mu s + [(50°C - 25°C)(0.05\mu s/°C)] \\
&= 19.72\mu s
\end{aligned}
$$

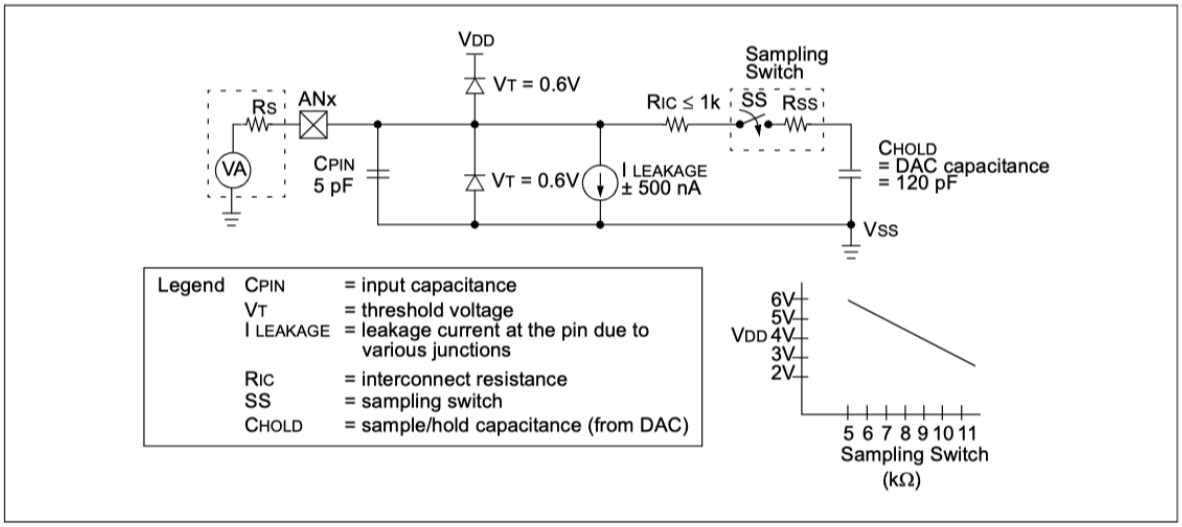
Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

4: After a conversion has completed, a 2.0TAD delay must complete before acquisition can begin again. During this time, the holding capacitor is not connected to the selected A/D input channel.

FIGURE 11-2: ANALOG INPUT MODEL



11.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires a minimum 12TAD per 10-bit conversion. The source of the A/D conversion clock is software selected. The four possible options for TAD are:

- 2TOSC
- 8TOSC
- 32TOSC
- Internal A/D module RC oscillator (2-6 μs)

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μs.

Table 11-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

TABLE 11-1: TAD vs. MAXIMUM DEVICE OPERATING FREQUENCIES (STANDARD DEVICES (C))

AD Clock Source (TAD)		Maximum Device Frequency
Operation	**ADCS1:ADCS0**	**Max.**
2TOSC	00	1.25 MHz
8TOSC	01	5 MHz
32TOSC	10	20 MHz
RC(1, 2, 3)	11	**(Note 1)**

Note 1: The RC source has a typical TAD time of 4 μs, but can vary between 2-6 μs.
2: When the device frequencies are greater than 1 MHz, the RC A/D conversion clock source is only recommended for SLEEP operation.
3: For extended voltage devices (LC), please refer to the Electrical Characteristics (Sections 15.1 and 15.2).

11.3 Configuring Analog Port Pins

The ADCON1 and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, any pin configured as an analog input channel will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

2: Analog levels on any pin that is defined as a digital input (including the AN7:AN0 pins), may cause the input buffer to consume current that is out of the device specifications.

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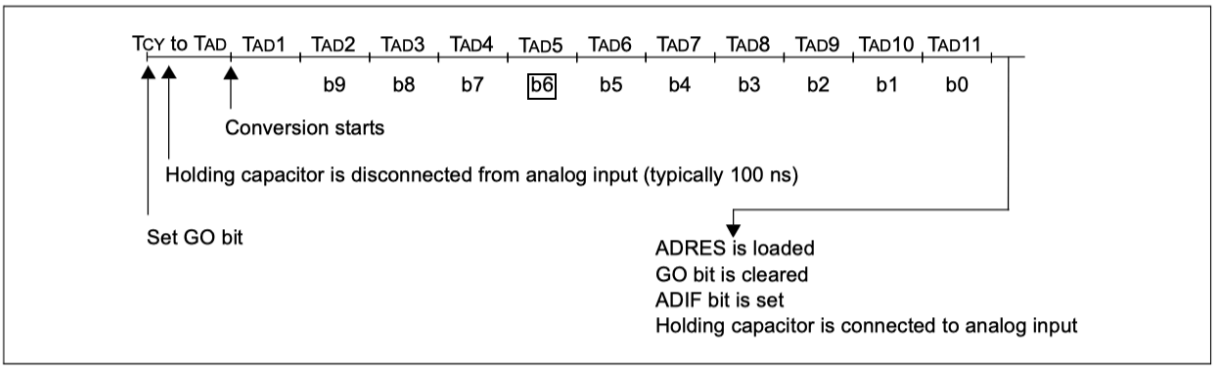
11.4 A/D Conversions

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D result register pair will NOT be updated with the partially completed A/D conversion sample. That is, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, acquisition on the selected channel is automatically started. The GO/$\overline{\text{DONE}}$ bit can then be set to start the conversion.

In Figure 11-3, after the GO bit is set, the first time segment has a minimum of TCY and a maximum of TAD.

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

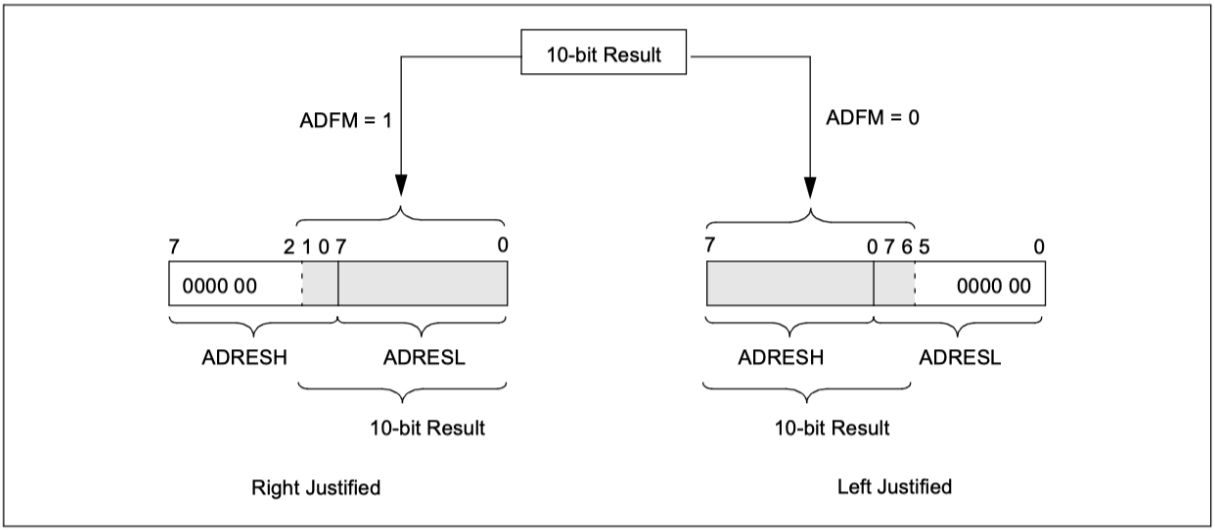
FIGURE 11-3: A/D CONVERSION TAD CYCLES



11.4.1 A/D RESULT REGISTERS

The ADRESH:ADRESL register pair is the location where the 10-bit A/D result is loaded at the completion of the A/D conversion. This register pair is 16-bits wide. The A/D module gives the flexibility to left or right justify the 10-bit result in the 16-bit result register. The A/D Format Select bit (ADFM) controls this justification. Figure 11-4 shows the operation of the A/D result justification. The extra bits are loaded with '0's'. When an A/D result will not overwrite these locations (A/D disable), these registers may be used as two general purpose 8-bit registers.

FIGURE 11-4: A/D RESULT JUSTIFICATION



11.5 A/D Operation During SLEEP

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed, the GO/DONE bit will be cleared and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To allow the conversion to occur during SLEEP, ensure the SLEEP instruction immediately follows the instruction that sets the GO/DONE bit.

11.6 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off, and any conversion is aborted. All A/D input pins are configured as analog inputs.

The value that is in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

TABLE 11-2: REGISTERS/BITS ASSOCIATED WITH A/D

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on MCLR, WDT
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	--0- 0000	--0- 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000	--0u 0000
89h(1)	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits			0000 -111	0000 -111
09h(1)	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx	---- -uuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: These registers/bits are not available on the 28-pin devices.

Document réponse :